ABSTRACT OF THE DISCLOSURE

It is an object of the present invention to reduce power consumption and improve flexibility in a master slice semiconductor integrated circuit. The master slice semiconductor integrated circuit comprises at least two wiring layers to form wirings, and a plurality of clock buffers connected by clock wirings in the form of a clock tree having at least two cascaded stages to distribute clock signals to a plurality of sequential circuits, wherein the clock wirings comprises a wiring layer switching portion which switches a wiring layer from a lower wiring layer of the at least two wiring layers to an upper wiring layer of the at least two wiring layers and then switches from the upper wiring layer to the lower wiring layer.